MSP430F20xx Device Erratasheet

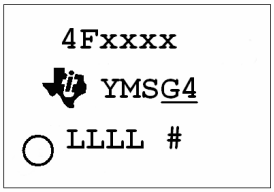
Current Version

Devices	Rev:	BCL9	BCL10	BCL11	CPU4	FLASH16	FLASH22	PORT10	SDA3	TA12	TA16	USI4
MSP430F2001	C	✓	✓	✓	✓	✓	✓	✓		✓	✓	
MSP430F2011	C	✓	✓	✓	✓	✓	✓	✓		✓	✓	
MSP430F2002	C	✓	✓	✓	✓	✓	✓	✓		✓	✓	✓
MSP430F2012	C	✓	✓	✓	✓	✓	✓	✓		✓	✓	✓
MSP430F2003	D	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F2013	D	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

Note: See Appendix for prior revisions

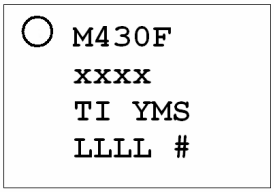
Package Markings

PW14: TSSOP(PW) 14-pin



YM = Year and Month Date Code
LLLL = LOT Trace Code
S = Assembly Site Code
# = DIE Revision
o = PIN 1

RSA16: QFN(RSA) 16-pin



YM = Year and Month Date Code
LLLL = LOT Trace Code
S = Assembly Site Code
# = DIE Revision
o = PIN 1

N14: PDIP(N) 14-pin

YM = Year and Month Date Code
LLLL = LOT Trace Code
S = Assembly Site Code
# = DIE Revision

Detailed Bug Description

BCL9 BCL9 – Bug description

Module: BasicClock, Function: ACLK divider modifications require delay before entering LPM3

After modifying the DIVAx bits, immediately entering LPM3 can cause the modification to be ignored and the divider settings not to take effect. Reading back the DIVAx bits will indicate the intended setting even when the divider has not been correctly applied.

Workaround:
When the DIVAx bits are modified, a delay of one complete ACLK (VLO or LFXT1CLK) period must elapse before entering LPM3. The delay is only necessary the first time LPM3 is entered after the DIVAx bits are modified. After the one-period delay, LPM3 may be entered and exited normally without additional delays.

BCL10 BCL10 – Bug description

Module: BasicClock, Function: MCLK = ACLK and P2SEL control bits

When using ACLK as the CPU MCLK clock source, the oscillator failsafe feature does not automatically switch MCLK to the DCO if the P2SEL6 or P2SEL7 bits are cleared. This applies when ACLK = LFXT1 (e.g. external low frequency clock source). The CPU will halt operation since no MCLK signal is present.

Workaround:
None

BCL11 BCL11 – Bug description

Module: BasicClock, Function: Watchdog failsafe when using ACLK

When using ACLK as the WDT+ clock source, the WDT+ oscillator failsafe feature does not automatically switch to the DCO if the P2SEL6 or P2SEL7 bits are cleared. This applies when ACLK = LFXT1 (e.g. external low frequency clock source). The WDT+ will halt operation since no clock signal is present.

Workaround:
None

CPU4 CPU4 - Bug description:

Module: CPU, Function: PUSH #4, PUSH #8

The single operand instruction PUSH cannot use the internal constants (CG) 4 and 8. The other internal constants (0, 1, 2, -1) can be used. The Assembler version 1.08 and higher produces correct code. The number of clock cycles is different:
PUSH #CG uses address mode 00, requiring 3 cycles, 1 word instruction
PUSH #4/#8 uses address mode 11, requiring 5 cycles, 2 word instruction

Workaround implemented in assembler.
No fix planned.

Detailed Bug Description (continued)

FLASH16 FLASH16 - Bug description:

Module: Flash, Function: Modifying INFOA addresses when LOCKA = 1 will modify main flash memory

When attempting to write to an address location, or perform a segment erase of INFOA while the LOCKA bit is set, flash memory beginning at main memory location 0xF040 and extending for 64 bytes to address 0xF07F will be modified erroneously. These 64 bytes are addressed and modified in place of the INFOA addresses when writes or erases are performed within the INFOA address space AND LOCKA = 1.

Workaround:
Prior to modifying (writing or erasing) any address within the INFOA Flash memory segment, properly clear the LOCKA control bit as described in the MSP430x2xx User's Guide to unlock the segment. Once the modification is complete, setting the LOCKA bit is recommended.

FLASH22 FLASH22 – Bug description

Module: Flash, Function: Flash controller may prevent correct LPM entry

When ACLK (or SMCLK) is used as the Flash controller clock source, and this clock source gets deactivated due to a low-power mode entry while a Flash erase or write operating is pending, the Flash controller will keep ACLK (or SMCLK) active even after the Flash operation has been completed. This will result in an incorrect LPM entry and increased current consumption. Note that this issue can only occur when the Flash operation and the low-power mode entry are initiated from code located in RAM.

Workaround:
Do not enter low-power modes while Flash erase or write operations are active. Wait for the operation to be completed before entering a low-power mode.

PORT10 Port10 - Bug description:

Module: Digital I/O, Function: Pull-up/down resistor selection when module pin function is selected

When the pull-up/down resistor for a certain port pin is enabled (PxREN.y=1) and the module port pin function is selected (PxSEL.y=1), the pull-up/down resistor configuration of this pin is controlled by the respective module output signal (Module X OUT) instead of the port output register (PxOUT.y).

Workaround:
None. Do not set PxSEL.y and PxREN.y at the same time.

SDA3 SDA3 - Bug description:

Module: SD16_A, the interrupt delay function can result in incorrect conversion data

The interrupt delay operation can result in incorrect conversion data when SD16INTDLYx = 01, 10 or 11.

Workaround:
Use SD16INTDLYx = 00 setting (Interrupt generated after 4th conversion). This will apply to the first conversion in Continuous mode and to each conversion in Single mode.

Detailed Bug Description (continued)

TA12 TA12 - Bug description:

Module: TimerA, Function: Interrupt is lost (slow ACLK)

TimerA counter is running with slow clock (external TACLK or ACLK) compared to MCLK. The compare mode is selected for the capture/compare channel and the CCRx register is incremented by 1 with the occurring compare interrupt (if TAR = CCRx).
Due to the fast MCLK the CCRx register increment (CCRx = CCRx+1) happens before the TimerA counter has incremented again. Therefore the next compare interrupt should happen at once with the next TimerA counter increment (if TAR = CCRx + 1). This interrupt gets lost.

Workaround:
Switch capture/compare mode to capture mode before the CCRx register increment. Switch back to compare mode afterwards.

TA16 TA16 - Bug description:

Module: TimerA, Function: First increment of TAR erroneous when IDx > 00

The first increment of TAR after any timer clear event (POR/TACLR) happens immediately following the first positive edge of the selected clock source (INCLK, SMCLK, ACLK or TACLK). This is independent of the clock input divider settings (ID0, ID1). All following TAR increments are performed correctly with the selected IDx settings.

Workaround:
None

USI4 USI4 - Bug description:

Module: USI, Function: I2C Slave mode can generate a glitch at SCL

USI I2C Slave Operation at slower communication rates < 20kbps. During I2C Bus Active operation, if USICNT is written while SCL is high, I2C module will generate a glitch on SCL that can corrupt the I2C bus sequence.

Workaround:
Verify that SCL is low before writing USICNT register.

Appendix: Prior Versions

Devices	Rev:	BCL9	BCL10	BCL11	CPU4	FLASH16	FLASH22	PORT10	SBW1	SDA2	SDA3	TA12	TA16	TA17	USI1	USI2	USI3	USI4
MSP430F2001	C	✓	✓	✓	✓	✓	✓	✓				✓	✓					
	B	✓	✓	✓	✓	✓	✓	✓				✓	✓					
	A	✓	✓	✓	✓	✓	✓	✓	✓			✓	✓	✓				
MSP430F2011	C	✓	✓	✓	✓	✓	✓	✓				✓	✓					
	B	✓	✓	✓	✓	✓	✓	✓				✓	✓					
	A	✓	✓	✓	✓	✓	✓	✓	✓			✓	✓	✓				
MSP430F2002	C	✓	✓	✓	✓	✓	✓	✓				✓	✓					✓
	B	✓	✓	✓	✓	✓	✓	✓				✓	✓					✓
	A	✓	✓	✓	✓	✓	✓	✓	✓			✓	✓					✓
MSP430F2012	C	✓	✓	✓	✓	✓	✓	✓				✓	✓					✓
	B	✓	✓	✓	✓	✓	✓	✓				✓	✓					✓
	A	✓	✓	✓	✓	✓	✓	✓	✓			✓	✓					✓
MSP430F2003	D	✓	✓	✓	✓	✓	✓	✓			✓	✓	✓					✓
	C	✓	✓	✓	✓	✓	✓	✓			✓	✓	✓					✓
	B	✓	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F2013	D	✓	✓	✓	✓	✓	✓	✓			✓	✓	✓					✓
	C	✓	✓	✓	✓	✓	✓	✓			✓	✓	✓					✓
	B	✓	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓

Detailed Bug Description

SBW1 SBW1 - Bug description:

Module: Spy Bi-Wire-Interface

An error in the Spy Bi-Wire-Interface will increase the ICC under normal operating conditions.

Workaround:
None

SDA2 SDA2 - Bug description:

Module: SD16_A, Internal reference generator is out of spec

The SD16_A reference generator may not meet the maximum temperature coefficient specification of 50 ppm/K.

Workaround:
The SD16_A internal reference can be adjusted to operate within the specification by writing 0x61 to memory location 0xBF. This will correct the temperature coefficient of the internal reference and center the typical voltage to 1.20V.

Detailed Bug Description (continued)

TA17 TA17 - Bug description:

Module: TimerA, Function: Capture Input CCIOB missing ACLK connection

The TimerA Capture Input CCI0B is not internally connected to the ACLK signal.

Workaround:
The ACLK signal can be output on P1.0 and externally input on a TimerA capture input pin.

USI1 USI1 - Bug description:

Module: USI, Function: USICKCTL cannot be written

When the USI is in active operation mode i.e. when USICNT <> 0, the USICKCTL cannot be written. If written, the USICNT is cleared and the USIIFG is set. Operation using the USISWCLK is not possible.

Workaround:
None

USI2 USI2 - Bug description:

Module: USI, Function: I2C Slave mode erroneously pulls SCL low

When the USI is configured in I2C slave mode, SCL will incorrectly be pulled low when USICNTx is written with a value of 1.

Workaround:
None

USI3 USI3 - Bug description:

Module: USI, Function: I2C Slave mode does not hold SCL low

When the USI is configured in I2C slave mode, the module does not hold SCL low while USISTTIFG = 1 following a start condition.

Workaround:
None

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